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10/791,023	03/02/2004	Andrew G. Tucker	03226/361001; SUN040137	1283

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EXAMINER	
KHATRI, ANIL	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/791,023	TUCKER, ANDREW G.	
	Examiner	Art Unit	
	Anil Khatri	2191	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03/02/04* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 5, 8, 10-11, 13-15 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by *Bryg et al* USPN 6,430,670.

Regarding claims 1, 8, 13 and 20

Bryg et al teaches,

generating an interposing library comprising a first modified interface, wherein the first modified interface is dependent on a native page size (column 4, lines 9-19, FIG. 2 shows the process of mapping a virtual address into a physical address. Each virtual address is composed of three fields: the virtual region number (VRN) 12, the virtual page number (VPN) 13, and the page offset 14. The upper 3-bits select the virtual region number 12. The least-significant bits form the page offset 14. The virtual page number 13 consists of the remaining bits. The VRN bits 12 are not included in the VPN 13. The page offset bits 14 are passed through the translation process unmodified. Exact bit positions for the page offset and VPN bits vary depending on the page size used in the virtual mapping);

intercepting a call into a kernel by the interposing library, wherein the call is dependent on a non-native page size (column 2, lines 51-54, An alternate embodiment provides an apparatus and method for implementing a hardware VHPT walker that can, without software intervention, resolve a TLB-miss by looking up the mapping in the VHPT);

modifying the call using the first modified interface to obtain a modified call (column 9, lines 34-44, accessing an instruction at a virtual address 11 (FIG. 1) occurs at step 151. Next, it is determined if the virtual address 11 is implemented at step 152. If the virtual address 11 resolved is not implemented, process flows to an unimplemented instruction address trap at step 153. If the virtual address 11 desired is implemented, a search of the TLB 23 is performed at step 154. If the search of the TLB 23 at step 154 results in a entry being found, the process proceeds to step 171 with a fault check on the entry. If there is no fault detected at step 171, the memory is accessed at step 173. If a fault is detected, a memory access fault is raised for processing at step 172); and

generating a response to the modified call by the kernel using the native page size (column 8, lines 4-38, The hash function 131 is reversible if using the hash result and all but one input produces the missing input as the result of the reverse hash function. The easiest hash function and reverse hash function is a simple XOR of bits. To ensure uniqueness, software must follow these rules: 1. The minimum long format VHPT size is 32K bytes (1024 entries). 2. Software should use only one preferred page size for each unique region identifier, otherwise processor operation is undefined. 3. All tags for translations within a given region, must be created with

the preferred page size assigned to the region, otherwise processor operation is undefined. 4. Software is not allowed to have pages in the VHPT 40 that are smaller than the preferred page size for the region, otherwise processor operation is undefined. Software can specify a page with a page size larger than the preferred page size in the VHPT, but tag values for the entries representing that page size must be generated using the preferred page size assigned to that region).

Regarding claims 2, 3, 10, 11,14 and 15

Bryg et al teaches,

generating the call into the kernel by a user-level application. (column 6, lines 27-48, his bit is used to indicate the mapped physical page is not resident in physical memory. The memory attribute 82 (MA) describes the cacheability, coherence, write policy and speculative attributes of the mapped physical page. Access bit (A) 83 when deasserted, triggers an instruction or data access bit fault on reference for tracing or debugging purposes. Dirty bit (D) 84 when deasserted causes any store or semaphore reference to the page to cause a dirty bit fault. The privilege level (PL) 85 specifies a privilege level or promotion level of the page and controls using four levels of privilege. Privilege level zero is the most privileged and has access to all privileged instructions. Privilege level three is the least privileged. Access rights 86 (AR) is also used in page granular read right and execute permission and privilege controls. The physical page number (PPN) 87 provides the most significant bits of the mapped physical address depending on the page size used in the mappings. Reserve area 88 is a reserved for later utilization, and

user implemented space number 91 is left for specific user functionality definition. When exception deferral number (ED) 89 is asserted, a fault on the speculative load is forced to indicate a deferred exception).

Regarding Claim 5

Rejection of claim 1 is incorporated and further claim recites limitation as in claim 1, therefore, claim 5 is rejected under same rationale.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4, 7, 9, 12 and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Bryg et al* USPN 6,430,670 in view of Earl et al USPN 5,815,686.

Regarding claims 4, 16 and 19

Berg et al teaches,

Page size but does not teach explicitly setting the non-native page size. However, Earl et al teaches (column 8, lines 31-52, the present invention treats the emulated virtual address differently from the native virtual address in the case of a TLB miss. For the emulated

virtual address 70, when there is a TLB miss, the present invention follows a TLB miss emulated procedure. In this procedure, the present invention accesses the translation table 78 and performs an associative look-up, as described above, to return a native virtual page number. The native virtual page number is indexed in the page table data structure 69 and a PFN 63 is returned. The present invention then stores the emulated virtual page number 79 and its corresponding PFN 63 as a TLB entry 66 in the TLB 61 (the "emulated procedure"). Thus, on a subsequent access to the same emulated virtual address 70, the PFN 63 is returned from the TLB 61 and concatenated with the offset 68 to form the physical address 64. It should be appreciated that the present invention uses 64 bit addressing (40 significant bits) in an otherwise 32 bit emulator. Native 32 bit addresses in the MIPS architecture are really 64 bit addresses with the higher order bits being zero. The present invention essentially maps a 32 bit x86 virtual address space into a portion of the 64 bit MIPS native virtual address space). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made to incorporate non-native page size for processing. The modification would have been obvious because one of ordinary skill in the art would have been motivated to combine teaching into utilizing both native and non native page sizes for translation in virtual environment.

Regarding claims 6, 9, 12, 17 and 18

Earl et al teaches,

searching a plurality of interfaces to determine which of the plurality of interfacesinclude the native page size (columns 7-8, lines 64-67 and 1-9, Referring now to FIG. 7, the data structure

representing the virtual to physical address space translation is shown. FIG. 7 shows the virtual address 60 of FIG. 6 in more detail. In one embodiment, the native virtual address 60 has a 12 bit, or 4 Kbyte, page size labeled Offset 68. The remaining 20 bits of the address represent the virtual page number (VPN), and index a 1M-entry page table data structure (page table) 69 in main memory. The top 8 bits are the address space identifier (ASID). The native virtual address 60 translates into the physical address 64, where the page frame number (PFN) 63 is either returned from the TLB 61 (TLB hit), or from the page table 69 (TLB miss), and the offset 68 comes directly from the native virtual address 60.) ; and

modifying the plurality of interfaces that include the native page size to obtain a plurality of modified interfaces, wherein modifying the plurality of interfaces uses the non-native page size (column 9-10, lines 50-67 and lines 1-3, In the case of a TLB hit, in step 81, the TLB 61 immediately (typically two or less clock cycles) returns the page frame number corresponding to the virtual page number. As described above, the TLB 61 stores virtual page numbers with their corresponding page frame numbers regardless of whether the virtual page numbers are emulated virtual page numbers or native virtual page numbers. When the virtual page number has a match in the TLB 61, the corresponding page frame number is located and returned without costly software look-up routines. In step 82, the corresponding page frame number is located and returned and the process 900 ends in step 94. Thus, each time a previously accessed virtual page number is received, the process of the present invention executes steps 81, 82, and 94. Steps 81 and 82 are implemented in the CAM logic circuitry of the TLB 61 and execute within one or two clock cycles, as opposed to the costly software associative look-up

procedures of the prior art. This greatly increases the speed of applications running on the computer system 112. Thus, non-native applications run much faster using the process of the present invention).

Regarding claim 7

Earl et al teaches,

determining the page size dependency using the modified response (column 8, lines 53-63, the present invention determines whether the virtual address is an emulated virtual address or a native virtual address by examining the ASID 76. In one embodiment, if the ASID 76 is a non-zero value, it indicates the virtual address is an emulated virtual address, wherein the ASID 76 specifies which x86 address space must be accessed, and the TLB miss emulated procedure is followed. If the ASID 76 is a zero value, it indicates that the virtual address 70 is a native virtual address and the TLB miss native procedure is followed).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anil Khatri whose telephone number is 571-272-3725. The examiner can normally be reached on M-F 8:30-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wei Zhen can be reached on 571-272-3708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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ANIL KHATRI
PRIMARY EXAMINER